What is claimed is:

1. A shift and shift-out detecting circuit comprising:

a plurality of partial shift circuits which respectively have bit shift quantities different from each other, and are connected in series, wherein each of said plurality of partial shift circuits receives a shift result as a previous shift result from said partial shift circuit of a previous stage and a corresponding shift instruction, shifts said previous shift result by the corresponding bit shift quantity in response to said shift instruction to produce a current shift result, and outputs the current shift result to said partial shift circuit of a subsequent stage;

a plurality of shift-out detecting circuits which are respectively provided for said plurality of partial shift circuits, wherein each of said plurality of shift-out detecting circuits detects a shift-out of "1" bit from the current shift result and said corresponding shift instruction and generates a partial sticky signal when the shift-out is detected; and

a collecting circuit which collects said partial sticky signals from said plurality of shift-out detecting circuits and generates a sticky signal to indicate generation of the shift-out.

2. The shift and shift-out detecting circuit according to claim 1, wherein said plurality of partial shift circuits are connected in series in order of larger bit shift quantities.

3. The shift and shift-out detecting circuit according to claim 1, wherein said bit shift quantities are 2^n (n is an integer equal to or larger than 0).

4. The shift and shift-out detecting circuit according to claim 1, wherein said plurality of partial shift circuits are connected in series in order of smaller bit shift quantities.

5. The shift and shift-out detecting circuit according to claim 1, further comprising:

a relaying circuit which collects said partial sticky signals from predetermined ones of said plurality of shift-out detecting circuits to produce a new partial sticky signal and outputs the new partial sticky signal to said collecting circuit.

6. The shift and shift-out detecting circuit according to claim 5, wherein said bit shift quantities are 2^n (n is an integer equal to or larger than 0).

7. The shift and shift-out detecting circuit according to claim 1, wherein when said plurality of partial shift circuits are connected in series in order of smaller bit shift quantities, said partial sticky signal from said partial shift-out detecting circuit for said bit shift quantity of 1 bit is supplied to said relaying circuit via said partial shift-out detecting circuit for said bit shift quantity of 4 bits.

8. The shift and shift-out detecting circuit according to claim 1, wherein when said plurality of partial shift circuits are connected in series in order of larger bit shift quantities, said partial sticky signal from said partial shift-out detecting circuit for said bit shift quantity of 4 bits is supplied to said collecting circuit via said partial shift-out detecting circuit for said bit shift quantity of 2 bit.

9. A floating-point calculating circuit comprising:

a comparing and subtracting circuit which inputs a first exponent of a first floating-point number and a second exponent of a second floating-point number, and generates a shit instruction indicating a difference between said first and second

exponents;

a digit adjustment shift and shift-out detecting circuit which carries out a first shifting operation of one of a first mantissa of the first floating-point number and a mantissa of the second floating-point number in response to said shit instruction, and detects shift-out in said first shifting operation in parallel to said first shifting operation to generate a first sticky signal;

a first rounding process circuit which carries out a first rounding operation to the shifted mantissa in response to said first sticky signal when the shift-out is detected by said first shift-out detecting circuit; and

a summing circuit which inputs a first sign of the first floating-point number and a second sign of the second floating-point number, and adds the shifted mantissa and the non-shifted mantissa based on the first and second signs.

10. The floating-point calculating circuit according to claim 9, wherein said digit adjustment shift and shift-out detecting circuit comprises:

a plurality of partial shift circuits which respectively have bit shift quantities different from each other, and are connected in series, wherein each of said plurality of partial shift circuits receives a

shift result as a previous shift result from said partial shift circuit of a previous stage and a corresponding partial shift instruction of said shift instruction, shifts said previous shift result by the corresponding bit shift quantity in response to said shift instruction to produce a current shift result, and outputs the current shift result to said partial shift circuit of a subsequent stage, and said partial shift circuit of the first stage receives said one mantissa as the previous shift result and said partial shift circuit of the last stage outputs the current shift result as said shifted mantissa to said first rounding process circuit;

a plurality of shift-out detecting circuits which are respectively provided for said plurality of partial shift circuits, wherein each of said plurality of shift-out detecting circuits detects a partial shift-out of "1" bit from the current shift result and said corresponding partial shift instruction and generates a partial sticky signal when the partial shift-out is detected; and

a collecting circuit which collects said partial sticky signals from said plurality of partial shift-out detecting circuits and generates said first sticky signal to indicate generation of said first shift-out.

11. The floating-point calculating circuit according to claim 10, wherein said bit shift quantities are 2^n (n is an integer equal to or larger than 0).

12. The floating-point calculating circuit according to claim 10, wherein said plurality of partial shift circuits are connected in series in order of larger bit shift quantities.

13. The floating-point calculating circuit according to claim 10, wherein said plurality of partial shift circuits are connected in series in order of smaller bit shift quantities.

14. The floating-point calculating circuit according to claims 10, wherein said digit adjustment shift and shift-out detecting circuit further comprises:

a relaying circuit which collects said partial sticky signals from predetermined ones of said plurality of shift-out detecting circuits to produce a new partial sticky signal and outputs the new partial sticky signal to said collecting circuit.

15. The floating-point calculating circuit according to claim 14, wherein said bit shift

quantities are 2^n (n is an integer equal to or larger than 0).

16. The floating-point calculating circuit according to claim 11, wherein when said plurality of partial shift circuits are connected in series in order of smaller bit shift quantities, said partial sticky signal from said partial shift-out detecting circuit for said bit shift quantity of 1 bit is supplied to said relaying circuit via said partial shift-out detecting circuit for said bit shift quantity of 4 bits.

17. The floating-point calculating circuit according to claim 11, wherein when said plurality of partial shift circuits are connected in series in order of larger bit shift quantities, said partial sticky signal from said partial shift-out detecting circuit for said bit shift quantity of 4 bits is supplied to said collecting circuit via said partial shift-out detecting circuit for said bit shift quantity of 2 bit.

18. The floating-point calculating circuit according to claim 9, further comprising:

a normalization shift and shift-out detecting circuit which carries out a normalizing operation to

the summation result from said summing circuit, and detects a second shift-out to generate a second sticky signal;

a second rounding process circuit which carries out a second rounding operation to the normalized summation result in response to said second sticky signal when the shift-out is detected by said first shift-out detecting circuit; and

an exponent increasing and decreasing circuit which adds the first and second exponents.

19. The floating-point calculating circuit according to claim 18, wherein said normalization shift and shift-out detecting circuit comprises:

a plurality of partial shift circuits which respectively have bit shift quantities different from each other, and are connected in series, wherein each of said plurality of partial shift circuits receives a shift result as a previous shift result from said partial shift circuit of a previous stage and a corresponding partial shift instruction of said shift instruction, shifts said previous shift result by the corresponding bit shift quantity in response to said shift instruction to produce a current shift result, and outputs the current shift result to said partial shift circuit of a subsequent stage, and said partial shift circuit of the first stage receives said

summation by said summing circuit as the previous shift result and said partial shift circuit of the last stage outputs the current shift result as said normalized summation to said second rounding process circuit;

a plurality of shift-out detecting circuits which are respectively provided for said plurality of partial shift circuits, wherein each of said plurality of shift-out detecting circuits detects a partial shift-out of "1" bit from the current shift result and said corresponding partial shift instruction and generates a partial sticky signal when the partial shift-out is detected; and

a collecting circuit which collects said partial sticky signals from said plurality of partial shift-out detecting circuits and generates said second sticky signal to indicate generation of said first shift-out.

20. The floating-point calculating circuit according to claim 19, wherein said plurality of partial shift circuits are connected in series in order of larger bit shift quantities.

21. The floating-point calculating circuit according to claim 19, wherein said plurality of partial shift circuits are connected in series in

order of smaller bit shift quantities.

22. The floating-point calculating circuit according to claim 19, wherein said normalization shift and shift-out detecting circuit further comprises:

a relaying circuit which collects said partial sticky signals from predetermined ones of said plurality of shift-out detecting circuits to produce a new partial sticky signal and outputs the new partial sticky signal to said collecting circuit.

23. The floating-point calculating circuit according to claim 19, wherein said bit shift quantities are 2^n (n is an integer equal to or larger than 0).